UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,033	09/11/2003	Bruce Leroy Beukema	ROC920030095US1	5841

7590 02/16/2006

Robert R. Williams
IBM Corporation - Dept. 917
3605 Highway 52 North
Rochester, MN 55901

EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 02/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/660,033	BEUKEMA ET AL.	
	Examiner	**Art Unit**	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which form s the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-4 and 7 are rejected under 35 USC 103(a) as being unpatentable over US Pat. Pub. No. 2003/0223416 to Rojas et al. (Rojas) in view of US Pat. No. 5,953,746 to Crocker et al. (Crocker).

5. Per claim 1, Rojas discloses a method for implementing dynamic VL buffer reconfiguration (Fig. 6, dynamic reallocation of virtual lane buffer space; Paragraphs 46+ disclose dynamically changing buffers of virtual lanes) in a channel adapter (Fig. 5, block 406 is the channel adapter, since it directly interfaces as a channel between two remote elements) comprising steps of: communicating a current port buffer size (paragraph 44+ discloses a buffer pool of memory, Fig. 5, element 508, where each port has a specific buffer size, Fig. 3 shows each port 302x is associated with a virtual lane, Fig. 3, element 306x, where the virtual lane has a specific amount of memory that is adjusted, "…An SMP can, at any time, change the number of configured virtual lanes forcing a redistribution of the amount of memory allocated to each virtual lane. The state machine 512 controls this process…"; clearly each virtual lane size associated with each port is stored/communicated to the virtual lane); communicating a current port buffer size of each physical port on the channel adapter (Paragraph 45 state that memory to *each* of the virtual lanes are redistributed dynamically; Paragraph 52 disclose "…a virtual lane is checked to determine whether the data in an identified virtual lane is less than the new required size", hence the current port buffer size must be communicated for the comparison to occur; Fig. 6, element 622 show comparison of VL size, element 628 shows looping that goes through all the VLs); utilizing the communications of the current buffer size for change requests for adjusting the current buffers size for a specific port (Fig. 6, elements 602, 604, 618 and 620 all show change requests where the current buffer size is needed, element 622) and adjusting said current port buffer size for an associated physical port (Fig. 6, element 626 shows resizing the buffer size of the port; Paragraph 52). Note that Rojas shows in Fig. 5 a port that has multiple lanes. Paragraph 44 discloses "…a link 406 supports 1,2,4 or 8 virtual lanes 306…". In each

port, there is set aside a memory block (Fig. 5, element 508). Rojas discloses this size is known to the port in Paragraph 45, where this total size is required to determine the VL memory size, "...the amount of memory allocated to each virtual lane is initially determined by dividing the total size of the memory by the number of VL configured...". Thus, Rojas discloses distinctly, a port buffer size and a VL buffer size, both of which are "adjusted" when the redistribution of memory amongst the virtual lanes are performed. Further note, Rojas clearly states the controller (Fig. 5, element 510) associated with each port has registers that control the operations of the channel adapters (Paragraph 41).

Rojas does not disclose expressly registers as the memory elements that storing data on buffer sizes of the port, virtual, channel adapter.

Crocker discloses registers (Fig. 3, element 22-24) for the purposes of storing buffer size information (Column 4, lines 50-57).

Rojas and Crocker are analogous art because they are from similar problem solving area involving in storage of buffer size information.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to store buffer size information of each level of the channel adapter, e.g., adapter buffer size, port buffer size and VL buffer size, in registers.

The suggestion/motivation for doing so would have been to allow simple and quick handle on the buffer size information as well as the fact that it is well-known to one of ordinary skill to store changeable configuration information in registers.

Therefore, it would have been obvious to combine Rojas with Crocker to go with conventional digital logic design practices in storing configuration information in registers.

6. Per Claims 2-4 and 7, Rojas combined with Crocker disclose claim 1, wherein Rojas further discloses the buffer, Fig. 5, element 508 being operated on by a state machine such that the state machine controls the memory allocation of the buffer (Paragraph 45) hence being an allocation unit. Rojas discloses the controller, element 510, having a plurality of registers for controlling the links. While Rojas does not expressly disclose the registers being partitioned in to predefined fields, it is evident that there are multiple criteria associated with the buffer of the virtual lane, i.e., each virtual lane needs to have an address, size, current buffer size (as previously mentioned for use with comparison), etc., which is a matter of design choice in how the designer wishes to parse and access these information fields. Rojas further discloses comparison and update markers (Fig. 6, element 626), which is construed to be status markers, which conventionally would be stored in registers.

7. Claims 11-19 are rejected under 35 USC 103(a) as being unpatentable over Rojas in view of Crocker in further view of US Pat. Pub. No. 2003/0046505 to Craddock et al. (Craddock).

8. Per Claims 11 and 17, Rojas combined with Crocker discloses an apparatus and computer program product as spelled out above in Claim 1 for a different statutory category, but applied in parallel here. Rojas also discloses the state machine (Fig. 5, element 510) and controller (Fig. 5, element 512) being the control units for controlling registers and controlling buffer sizes (Paragraphs 41 and 45). Rojas further discloses an architecture (Fig. 2) where multiple hosts exist and share resources.

Rojas combined with Crocker does not disclose expressly a hypervisor being the operation unit that performs the changes made involving the registers and buffer size.

Craddock teaches a very similar architecture as Rojas (Fig. 1, has multiple hosts as end nodes connected via the same switch and router scheme; Fig. 3B shows the same high-level virtual lane diagram that Rojas discloses) the use of hypervisors in order to allow multiple hosts with multiple operating systems to be virtualized and share hardware resources (paragraph 124).

Rojas combined with Crocker, and Craddock, are analogous art because they are from the same field of endeavor in virtual lane buffering in what appears to be identical applications in a system architectural context.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement the overall control of the buffering size, registers, status of the channel adapter with the hypervisor.

The suggestion/motivation for doing so would be that it is natural for the central control unit that enables multiple disparate hosts to communicate with each other over virtual lanes to control the buffering, registers and channel adapter associated with the virtual lanes.

Therefore, it would have been obvious to combine Rojas and Crocker with Craddock for the benefit of centralized control of virtual lane hardware/software.

9. Per Claims 12,13,15 and 19, Examiner applies the rejections of Claim 2-4 and 7 based on the similarity of the claims and the additional teachings of Rojas.

10. Per Claims 14, 16 and 18, Rojas combined with Crocker and Craddock disclose claims 11 and 17, wherein Rojas further discloses having a buffer state machine (Fig. 5, element 512) that performs various monitoring and control operations on the VL buffers (Paragraphs 44+).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patents and patent related publications are cited in the Notice of References Cited (Form PTO-892) attached to this action to further show the state of the art with respect to virtual lane buffering.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
02/09/2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
2/10/06